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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/580,223	05/26/2000	Andrew Kay	YAMAP0713US	8243

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Neil A DuChez
Renner Otto Boisselle & Sklar LLP
19th Floor
1621 Euclid Avenue
Cleveland, OH 44115

EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	10

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/580,223	KAY ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-13 of U.S. Application 09/580,223 filed on 05/26/2000 are presented for examination. The application claims foreign priority to U.K. Patent Application 9912232.7, dated 05/27/1999. Applicants' paper #9 is a Request for Reconsideration. No amendments to the claims are made in paper #9.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. More specifically, the lines, numbers ~~an~~ and letters are not uniformly thick and well defined, as required by 37 CFR 1.84(i). Formal drawings will be required when the application is allowed.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).
5. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).
6. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claim a compiler for a hardware description language that "... is arranged to retime the synchronized communication without changing the order of external communication of the integrated circuit ..." (Claim 1 of issued patent). The instant application describes it as "...the method uses a language construct which effects synchronized communication between the sender process and the receiver process.
7. Claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not

patentably distinct from each other because the "...hardware optimizer is arranged to perform scheduling and allocation" in the issued claim is functionally equivalent to "pre-emptive scheduler" in the instant application.

8. Claim 3 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because the issued claim refers to "... retime the synchronized communication without changing the order ...". This is functionally equivalent to "... the send algorithm is carried out without descheduling" in the instant application.
9. Claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because the issued claim uses the term "handshaking", which is the term commonly used in the art for "... a check that all of the receiver processes are ready to receive data before data is transferred ...." (Claim 4 of the instant application).
10. Claim 5 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

a. the "...hardware optimizer is arranged to perform scheduling and allocation" in the issued claim is functionally equivalent to "pre-emptive scheduler" in the instant application.

b. the issued claim uses the term "handshaking", which is the term commonly used in the art for "... a check that all of the receiver processes are ready to receive data before data is transferred ...." (Claim 4 of the instant application).

11. Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because the issued claim refers to "... retime the synchronized communication without changing the order ...". This is functionally equivalent to "... the receive algorithm is carried out without descheduling" in the instant application.

12. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because the issued claim teaches "... wherein the compiler includes a hardware optimizer for optimizing hardware implementation ...". This is equivalent to the claim in the instant application for "... at one of said processes is embedded in hardware."

13. Claim 8 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because the issued claim teaches "... defining functions of the integrated circuit in a programming language ...wherein the compiler includes a hardware optimizer for optimizing hardware implementation ...". This is equivalent to the claim in the instant application for "... all of said processes are described in said hardware description language."

14. Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because the issued claim teaches "... defining functions of the integrated circuit in a programming language ...wherein the compiler includes a hardware optimizer for optimizing hardware implementation ...". This is equivalent to the claim in the instant application for "... first simulating at least part of the circuit ... then creating the circuit using said hardware compiler."

15. Claim 10 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 10 of U.S. Patent No. 6,021,266. Although the conflicting claims are not identical, they are not patentably distinct from each other because the issued claim teaches "An integrated circuit which is designed by the method according to claim 1." This is

equivalent to the claim in the instant application for "A synchronous electrical circuit as claimed in claim 9, which is a digital electronic circuit."

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. The prior art used for these rejections is as follows:

18. Kay, Andrew, U.K. Patent Application 2,317,245. Date of Publication: March 18, 1998. (Henceforth referred to as "**Kay**").

19. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

20. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kay.

21. In regards to Claim 1, Kay teaches the following limitations:

1. A method of transferring data from a sender process to a plurality of receiver processes,
(Kay, especially: Fig.2C and associated text; p.6, 4th para.; Claim 1; p.15, last para.)

wherein at least one of said processes is described in a hardware description language,
(Kay, especially: Fig.1, Items 1,7,11; p.9, lat para.; p.15, last para; p.23, para.3)

said hardware description language incorporating simulation means for simulation of the behaviour of hardware and also incorporating a hardware compiler for deriving hardware which behaves according to said simulation,
(Kay, especially: Fig.1, Items 9,10; pp.22-23)

characterised in that the method uses a language construct which effects synchronised communication between the sender process and the receiver processes.
(Kay, especially: Fig.1, Items 9,10; pp.22-23; Figs.2A-2C; pp.24-25)

22. In regards to Claim 2, Kay teaches the following limitations:

2. A method as claimed in claim 1 which involves carrying out a send algorithm under the control of a pre-emptive scheduler.
(Kay, especially: Fig.1, Items 9,10; pp.22-23; Figs.2A-2C; pp.24-25)

23. In regards to Claim 3, Kay teaches the following limitations:

3. A method as claimed in claim 2 , characterised in that the scheduler ensures that the send algorithm is carried out without descheduling.
(Kay, especially: Fig.1, Items 9,10; pp.22-23; Figs.2A-2C; pp.24-25)

24. In regards to Claim 4, Kay teaches the following limitations:

4. A method as claimed in claim 2, characterised in that a check is made that all of the receiver processes are ready to receive data before data is transferred from the sender process to the receiver processes.
(Kay, especially: Fig.1, Items 9,10; pp.22-23; Figs.2A-2C; pp.24-25)

25. In regards to Claim 5, Kay teaches the following limitations:

5. A method as claimed in claim 1 which involves carrying out a receive algorithm under the control of a pre-emptive scheduler.
(Kay, especially: Fig.1, Items 9,10; pp.22-23; Figs.2A-2C; pp.24-25)

26. In regards to Claim 6, Kay teaches the following limitations:

6. A method as claimed in claim 5, characterised in that the scheduler ensures that the receive algorithm is carried out without descheduling.
(Kay, especially: Fig.1, Items 9,10; pp.22-23; Figs.2A-2C; pp.24-25)

27. In regards to Claim 7, Kay teaches the following limitations:

7. A method as claimed in claim 1, characterised in that at least one of said processes is embodied in hardware.
(Kay, especially: Fig.1, Items 9-12; pp.22-23; Figs.2A-2C; pp.24-25)

28. In regards to Claim 8, Kay teaches the following limitations:

8. A method as claimed in claim 1, characterised in that all of said processes are described in said hardware description language.
(Kay, especially: Fig.1, Items 9-12; pp.22-23; Figs.2A-2C; pp.24-25)

29. In regards to Claim 9, Kay teaches the following limitations:

9. A synchronous electrical circuit produced by first simulating at least part of the circuit in accordance with the method of claim 1, and then creating the circuit using said hardware compiler.
(Kay, especially: Figs.3-10 and associated text)

30. In regards to Claim 10, Kay teaches the following limitations:

10. A synchronous electrical circuit as claimed in claim 9, which is a digital electronic circuit.
(Kay, especially: Figs.3-10 and associated text)

31. In regards to Claim 11, Kay teaches the following limitations:

11. A hardware description language adapted to simulate the behaviour of at least a sender process and a plurality of receiver processes, and comprising a language construct which effects synchronised communication between the sender process and the recciver processes.
(Kay, especially: Fig.1, Items 9-12 and associated text)

32. In regards to Claim 12, Kay teaches the following limitations:

12. A hardware description language adapted to carry out the method of claim 1.
(Kay, especially: Fig.1, Items 9-12 and associated text)

33. In regards to Claim 13, Kay teaches the following limitations:

13. A computer readable medium carrying a computer program adapted to carry out the method of claim 1.
(Kay, especially: Fig.1, Items 9-12 and associated text)

Response to Arguments

Re: Drawings

34. Examiner acknowledges Applicants statement (paper #9, p.2) that they will provide formal drawings if the application is allowed.

Re: Double Patenting

35. In paper #9, pp.2-4, Applicants unpersuasively argue that Claim 1 of the present application is not an obvious variation of Claim 1 in U.S. Patent 6,201,266 ("**Kay '266**").

36. In the first argument (Section "II.(a)", p.2), Applicants argue that

> "The present invention relates to a method of *transferring data* from a sender process to a plurality of receiver processes. Claim 1 of *Kay '266* is directed to method of *designing an integrated circuit*. The inventions are completely different."

Examiner respectfully disagrees. Applicants have only cited 2 words out of Claim 1 of the present application.

A more thorough reading of the claim shows that the present invention relates to "a method of transferring data from a sender process to a plurality of receiver processes, wherein at least one of said processes is described in *a hardware description language*, said hardware description language incorporating simulation means for *simulation of the behaviour of hardware* and also incorporating a hardware compiler *for deriving hardware which behaves according to said simulation*...." (See reproduction of the claim in paper #9, p.2).

As the Applicants note (paper #9, p.2), Claim 1 of the *Kay '266* patent relates to "a method of designing an integrated circuit." Examiner finds the "simulation of the behaviour of hardware" and the "deriving hardware which behaves according to said simulation" in the present application to be an obvious textual variation of the functionally equivalent "method of designing an integrated circuit" in *Kay '266*.

37. In the second argument (Section "II.(b)", pp.2-3), Applicants argue that

> "Claim 1 of the present application refers to at least one of the processes being described in a hardware description language. Claim 1 of *Kay '266* refers to 'defining functions of the integrated circuit in a programming language which supports parallelism and synchronized communication.' A 'process described in a hardware description language' is not substantially identical to a 'function defined in a programming language which supports parallelism and synchronized communication.' The inventions are completely different."

Examiner respectfully disagrees.

As the Applicant notes, Claim 1 of *Kay '266* refers to "defining functions of the integrated circuit in a programming language which supports parallelism and synchronized communication." *Kay '266* therefore limits the programming language to one which supports parallelism and synchronized communication. It is well known in the art that hardware definition languages have such features. Moreover, it is well known in the art that the programming languages best suited to "define functions of [an] integrated circuit" are hardware definition languages, which were created for this purpose.

Claim 1 of the present application refers to "processes being described in a hardware description language." Examiner finds the "processes being described in a hardware description language" in the present application to be an obvious textual variation of the functionally equivalent "defining functions of the integrated circuit in a programming language which supports parallelism and synchronized communication" in *Kay '266*.

38. In the third argument (Section (Section "II.(c)", p.3), Applicants argue that

> "Claim 1 of the present application refers to the hardware description language incorporating simulation means for simulation of the behaviour of hardware and also incorporating a hardware compiler for deriving hardware which behaves according to said simulation. Claim 1 of *Kay '266* refers to *applying* a compiler which is arranged to retime the synchronized communication without changing the order of external communication, etc. Applicants note that 'applying a compiler' is not substantially the same invention as 'hardware description language incorporating simulation means for simulation of the behaviour of hardware and also incorporating a hardware compiler for deriving hardware which behaves according to the simulation.' Again, the inventions are completely different."

Examiner respectfully disagrees.

As the Applicant notes, Claim 1 of *Kay '266* refers to "*applying* a compiler". In addition, Claim 1 of *Kay '266* also refers to "wherein the compiler includes a hardware optimizer for optimizing hardware implementation which is represented by the output code."

Claim 1 of the present invention refers to "incorporating a hardware compiler for deriving hardware which behaves according to said simulation." Examiner finds the descriptions of the compilers in the two claims to be obvious textual variations of the same element – the use of a compiler in a method claim.

39. In the fourth argument (Section (Section "II.(d)", p.3), Applicants argue that

> "Claim 1 of the present application refers to the method using a 'language construct which effects synchronized communication between the sender process and the receiver processes.' Claim 1 of *Kay '266* refers to 'applying a compiler which is arranged to retime the synchronized communication without changing the order of external communication.' A 'language construct which affects synchronized communication between the sender process and the receiver processes' is not substantially the same invention as 'applying a compiler which is arranged to retime the synchronized communication without changing the order of external communication."

Examiner respectfully disagrees.

As the Applicant notes, Claim 1 of the present application refers to "the method uses a language construct which effects synchronized communication between the sender process and the receiver processes." Claim 1 also refers to "incorporating a hardware compiler for deriving hardware which behaves according to said simulation."

It is inherent that a "language construct" alone cannot "effect" synchronized communication in an IC design. A compiler is required in order to "derive hardware which behaves according to" the higher level "language construct".

Claim 1 of *Kay '266* refers to "applying a compiler which is arranged to retime the synchronized communication without changing the order of external communication." *Kay '266* is claiming a narrow implementation of "deriving hardware which behaves according to said simulation", where there is "a language construct which effects synchronized communication between the sender process and the receiver processes" (the language of Claim 1 in the present application).

Examiner finds the descriptions of the compilers in the two claims to be obvious textual variations of the same element – deriving hardware which behaves according to said simulation", where there is "a language construct which effects synchronized communication between the sender process and the receiver processes."

40. Examiner is therefore maintaining the double patenting rejection of Claim 1 on the basis of *Kay '266*. Examiner is also maintaining the rejections of dependent claims 2-10, which have not been traversed (but not argued) by the Applicants in paper #9.

Re: Claim Rejections - 35 USC § 102

41. Applicants note that the reference used in the 35 USC §102(b) rejections, UK Patent App. 2,317,245 (henceforth "*Kay '245*"), is the priority document for the *Kay '266* reference used in the double patenting rejections. Therefore, Applicant

is applying arguments presented against the *Kay '266* reference apply against the *Kay '245* reference as well.

42. More specifically, Applicants argue that the invention in the present application and the invention in *Kay '245* are different inventions, as argued in regards to the double patenting rejections. Examiner did not find these arguments to be persuasive. Examiner refers the Applicants to the responses above (paragraphs 35-40).

43. In addition, Applicants argue (paper #9, p.4) that:

> "*Kay '245* does not teach or suggest such "one-to-many" type of send-receive communication as recited in present claims 1 and 11. Rather, *Kay '245* teaches only a 'one-to-one' type of send-receive communication. Each send is matched by only one receive. There is no construct for effecting synchronized communication between a sender process and a plurality of receiver processes."

Applicants are referred to Fig.2c in both the *Kay '245* and the *Kay '266* references, as well as the text associated with the figures (*Kay '266*: col.12, lines 35-52. *Kay '245*: p.25). The text teaches that "All the other slave processes 21 wait for the master process to start before starting themselves. At the end of the parallel section, the master process 20 waits for all the slave processes 21 to finish before continuing itself." Inherent in this teaching are "one-to-many" and "many-to-one" types of send-receive communication.

44. Applicants also argue (paper #9, p.5) that:

> "Furthermore, regarding claims 5 and 6, the Examiner appears to believe that the terms 'pre-emptive scheduling' and 'descheduled' are related to the scheduler mentioned in *Kay '245*. However, in claims 5 and 6 of the present application, applicants are referring to statically scheduling hardware operations so that they will occur in particular clock cycles in the final product. In Kay '245, software simulation of a design is discussed using a 'pre-emptive scheduler' that is used to simulate a parallel design on a sequential computer by allocating time to each of the parallel components. Such 'scheduler' terminology is standard in both fields, however the terms are referring to different hardware/software operations in the present application and Kay '245, respectively."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., scheduling hardware operations as opposed to software processes) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

45. Applicants have not provided arguments in regards to the other rejections.

46. Examiner is therefore maintain all 35 USC §102(b) rejections.

Conclusion

47. Applicant's arguments filed in paper #9, on 9/19/03, have been fully considered but they are not persuasive.

48. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

All communications: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is:

(703) 305-3900.

Ayal I. Sharon

Art Unit 2123

November 14, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER